

RISK ASSESSMENT OF TRANSITION TO LEAD-FREE ELECTRONICS ASSEMBLY

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Abstract: The European Union's Restriction on Hazardous Substances (RoHS) Directive, imposed on electronics manufacturers in 2006, banned the use of certain toxic substances such as lead and cadmium in components and assemblies. Removal of lead which was used in solder, die attaches and surface finishes has introduced reliability risks such as thermo-mechanical fatigue, tin whiskers, tin pest, electro-chemical migration, and corrosion. Due to these concerns, certain reliability-critical industries such as medical, defense, and automotive were either exempted or excluded from these restrictions. Since the commercial electronics sectors have switched to lead-free materials, few suppliers now produce lead-based solders and surface finish boards. Hence there is a growing supply chain pressure on these exempted and excluded industries to switch to lead-free materials. However, they are hesitant to transition to lead-free due to previously said reliability concerns remaining with lead-free assemblies.

This study analyses possible failure modes and mechanisms to assess these reliability risks in this transition. The critical failure mechanisms included thermal and mechanical fatigue and tin whiskers. Simulation was conducted using CalcePWA software to compare the reliability between tin-lead and SAC305 solder under temperature cycling and vibration loading in addition to assessing the risk due to tin whiskers. The discussion is mainly focused on concerns about the changes in manufacturing practices, effects of storage and handling conditions on manufacturing defects, while susceptibility to other failure mechanisms are briefly discussed. The study provides assessment and important factors to be considered and monitored during lead-free transition.

Keywords: Lead-free, ENIG, Reliability, RoHS, Transition

Introduction: In 2003, the European Union (EU) passed the Restriction of Hazardous Substances (RoHS) directive limiting the use of certain hazardous substances in electrical and electronic equipment in EU member states and provided a mechanism for restricting additional substances in the future [1]. The RoHS directive (2002/95/EC) became effective on July 1, 2006, and was applicable to the ten categories of products listed in the WEEE directive, as well as to electric light bulbs and luminaires used in households. In particular, the RoHS 2 directive required medical devices and monitoring and control instruments to comply with current RoHS restrictions by July 2014 and industrial control and monitoring instruments to comply by July 2017. For all other equipment, unless explicitly excluded,

compliance is required by July 2019 [2]. The electrical and electronic equipment explicitly excluded were equipment used in military and space applications, large-scale stationary industrial tools, large-scale fixed installations, implantable medical devices, transportation applications (except for electric two-wheel vehicles), non-road mobile machinery, photovoltaic panels designed for permanent use, and equipment designed solely for the purpose of research and development [3].

With consumer electronics driving the trends in technology, the majority of electronic component manufacturers have already transitioned to the use of lead-free materials [4]. On the other hand, electronic manufacturers associated with aerospace, military, and space applications and that are excluded from government-imposed restrictions have generally attempted to maintain lead-based parts and assembly processes due to long-term reliability concerns with lead-free parts and assemblies. However, even some of these manufacturers have been investigating, and in some cases using, lead-free parts because they are the only parts that are affordable and available on the market. For example, it is nearly impossible to purchase high-density BGA packages in leaded versions [4]. As a result, manufacturers using tin-lead solder face the decision of assembling a lead-free BGA with tin-lead solder or replacing the lead-free solder balls on the BGA with tin-lead solder balls. Companies that have been excluded by the environmental legislation have been forced to make last-time buys and store spares or to use re-worked lead-free components. With potential reliability concerns from such re-worked assemblies as well as the risks associated with the inclusion of counterfeit components and the shrinking manufacturing base, these companies are now being compelled to evaluate the transition to lead-free materials.

This paper overviews the key reliability risks in transitioning to lead-free assembly. The intent is to address some of the reliability risks associated with process related to manufacturing, storage and handling of lead-free parts, but not to be an extensive analysis of any particular failure mechanism; the interested reader is referred instead to key references. Potential failure modes and mechanisms were studied to assess these reliability risks in the transition. Simulations were conducted to analyze risks of thermal, mechanical fatigue and tin whiskers in lead-free solders.

Analysis Sample Information: The board model used for simulated reliability assessment and risk assessment was an industrial controller board populated with integrated chips (ICs), resistors, capacitors (such as ceramic, electrolytic) and other standard electronic components used for controlling signals. Table 1 lists the materials that were considered for risk assessment through simulation and literature review:

Table 1 Materials Considered for Risk Assessment

	Lead-based Board	Lead-free Board
Solder Material	Sn63-Pb37	SAC305
Board Material	FR4	FR4

	Lead-based Board	Lead-free Board
Metallization Surface Finish	HASL (Hot Air Solder Leveling)	ENIG (Electroless Nickel Immersion Gold)

Table 2 outlines the potential failure modes and mechanisms of reliability concerns associated with lead-free manufacturing and operational practices. This is by no means the exhaustive list of all the problems with the usage of lead-free materials. But these are some of the most prominent reliability concerns. The failure mode here is broadly categorized as short and open circuits. The mechanisms are not listed based on risk priority as the effect, severity and frequency of occurrence depends on the application and lifecycle conditions the electronic packages are used in.

Table 2 Potential Failure Modes and Mechanisms of Lead-free Process

Potential Failure Site	Potential Failure Modes	Potential Failure Causes	Potential Failure Mechanisms
Plastic encapsulation of integrated chips (a-A)	(a) Open/parameter drift/intermittent	Reflow process, improper storage conditions	A. Popcorning
		Temperature cycling, power cycling, mechanical vibration	B. Solder cracks
High current density ($>10^4$ A/cm ²)/manufacturing defects		C. Electromigration	
Shock or vibration loading/poor handling, thermal cycling		D. Pad cratering	
Higher reflow temperature, poor flux		E. Solderability	
High temperature (>50 °C), salt content		F. Solder corrosion	
Impurities in resin, high reflow temperature, moisture ingress		G. Conductive anode filament	
Solder Joints (a-F)	(b) Short/parameter drift/intermittent	Humid conditions, voltage bias, contaminants	H. Dendrites/ Electrochemical migration
		Temperature cycling, humidity,	I. Tin whiskers
Plated through holes (b-G)			

Potential Failure Site	Potential Failure Modes	Potential Failure Causes	Potential Failure Mechanisms
Electrical connectors (b-I)		electroplating process, CTE mismatch b/w conductor and finish	

Reliability Risks: Some of the reliability risks mentioned in the above analysis are evaluated in the following section using literature review and simulation. The evaluation provides a comparison between tin-lead and lead-free packages in terms of possible risks associated with manufacturing, storage and usage of lead-free materials.

Solderability: Currently available lead-free solders have a solidus/liquidus point about 20-50°C higher (depending on the alloy) than the lead-based pastes currently in use [6]. The primary challenge lead-free solders will present electronics assemblers with is higher process temperatures. Minimizing process temperatures limits the thermal stress on boards and components, reducing the potential for manufacturing defects. Higher reflow process thermal cycles expose PCBs to significant amounts of stress on plated through holes and barrels, which can lead to cracking. Higher first pass temperatures on double-sided assemblies expose bottomside finished surfaces to oxidation or interdiffusion, which in turn can lead to solderability problems on the second pass.

Popcorning: Limiting peak temperatures limits intermetallic growth, especially on topside components that are exposed to two passes, and also limits the potential for the popcorning of components with high moisture content. Increasing the maximum reflow temperature is expected to increase the moisture sensitivity of plastic packaged components. Moisture diffusion in epoxy molding compounds (EMCs) is one of the major reliability concerns in plastic encapsulated microcircuits (PEMs), because many failure modes observed in these devices are believed to arise from the diffusion of moisture during manufacturing, storage, or operation [7]-[11]. Moisture desorption in EMCs takes place at reflow process. Moreover, it is important to understand the mechanism of moisture desorption, since during the assembly of PEMs, the packages undergo baking to remove moisture and thus reduce the probability of moisture-induced failures such as popcorn cracking and interfacial delamination. In the most severe case, the stress can result in external package cracks. This is commonly referred to as the “popcorn” phenomenon because the internal stress causes the package to bulge and then crack with an audible “pop” [12]. Plastic-encapsulated components have to be checked for their MSL (moisture sensitivity level) to find the maximum exposure time allowed outside the moisture-resistant bag during storage. Improper storage, handling, or packaging of plastic encapsulated semiconductor devices can allow the introduction of moisture. Moisture trapped inside plastic-encapsulated packages can damage them during soldering, as the moisture vaporizes and tries to expand. This internal vapor pressure can cause separation of the plastic package from the semiconductor chip or lead frame, internal or external cracks, and damage to thin films and wire bonds.

Simulation: The simulation of stress response of these boards under temperature cycling, vibrations, and susceptibility of these materials to tin whiskers were carried out using CalcePWA software. The CalcePWA software consists of a set of simulation tools that use various thermo-mechanical stress and damage models.

The model of the board with components assembled on it, as shown in Figure 1, was used for the simulation.

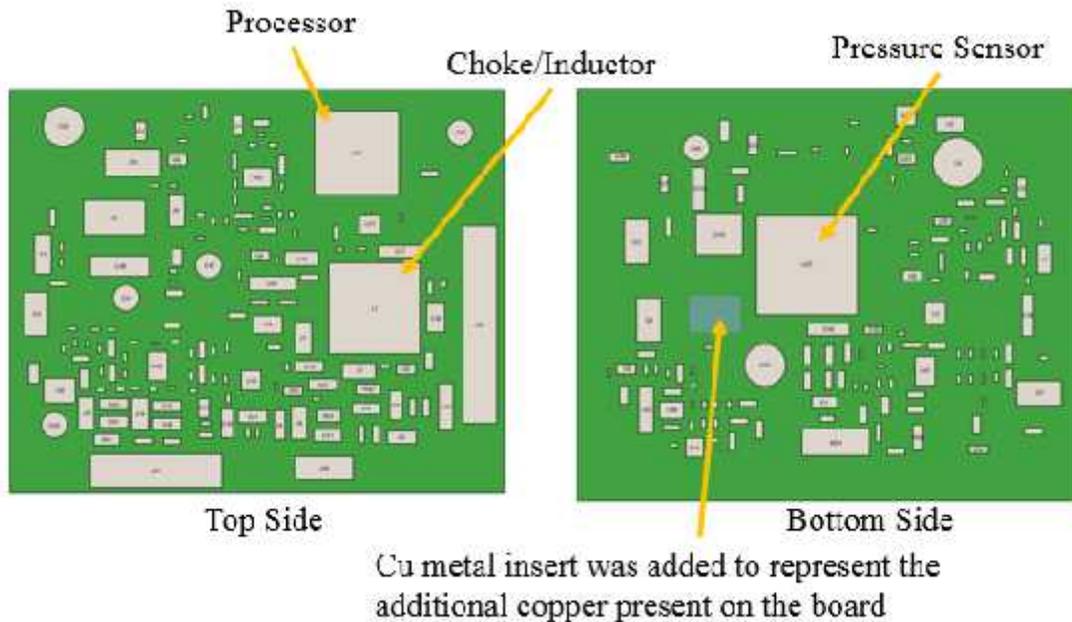


Figure 1 CalcePWA CAD Model of the Board with Components

Thermal analysis was conducted to determine the temperature gradient across the board and the temperature rise of the components under a given temperature. The power dissipation values of components, obtained from typical real-time applications, were taken up for analysis. No particular cooling solution was considered and hence conduction across board and natural vertical convection to the ambience was chosen as the heat transfer model. The thermal analysis was conducted for each extreme temperature that was to be used for the temperature cycling tests (shown in Table 3, Table 4). It was observed that certain ICs (transceivers-U15), fuse (F4), ceramic capacitors, ceramic diodes, and processor exhibited the highest rise in temperature of 17-18 °C (as shown in an example in Figure 2) during each thermal stress while many other components such as electrolytic capacitors, op-amps, and a few other ICs exhibited temperature rise of 3-5 °C.

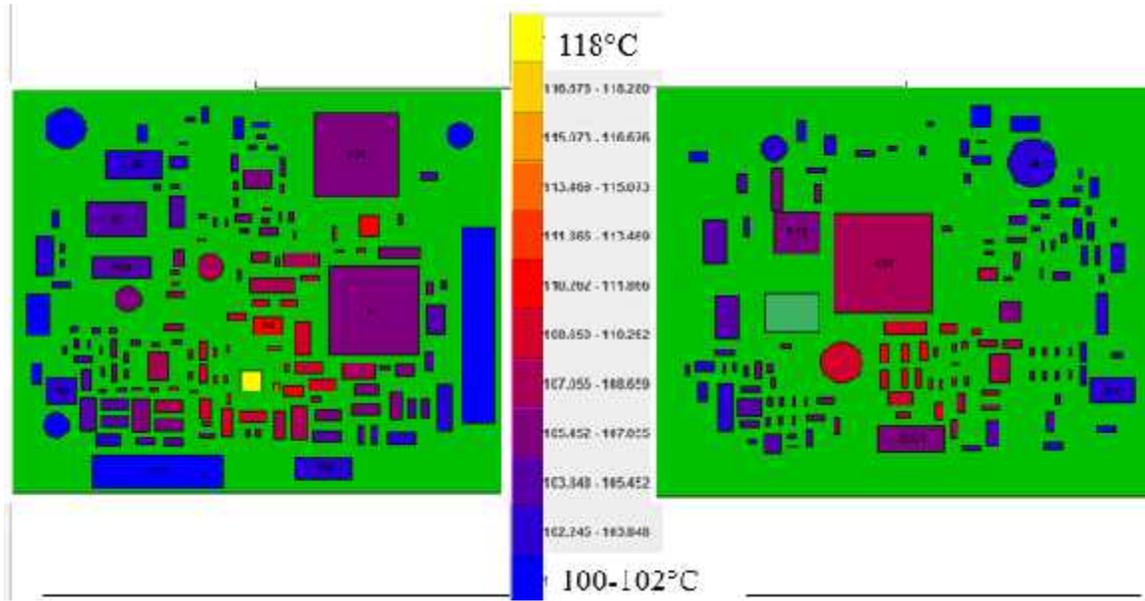


Figure 2 Temperature Distribution at 100 °C Ambient Temperature

Temperature cycling analysis was conducted to assess relative risks of interconnect failures for the components. Simulation test conditions were adapted from standards for accelerated temperature cycling. Temperature cycling was conducted for different conditions:

- Standard accelerated test as per JESD22-A104D [5] for 1000 cycles (Table 3 and Table 4).
- Assumed extreme real application conditions: Death Valley yearly temperature: Each of the temperature range was assumed to undergo 2 cycles per day and for 3 months continuously before the next temperature range starts. This condition was applied for a 10 year operating period.

The thermal analysis results obtained previously were used as inputs for each maximum and minimum temperature. Dwell time and ramp times were provided as shown in the Table 3 and Table 4.

Table 3 Temperature Cycling Condition as per JESD22-A104D

	Temp (°C)	Dwell Time (min.)
Minimum Temp.	0	10
Maximum Temp.	100	10
Ramp Time = 5mins		

Table 4 Temperature Cycling Condition Based on Death Valley Average Yearly Temperature

Temperature range	Dwell Time at max temp. (mins)	Dwell Time at min temp. (mins)	Ramp time (mins)	No. of cycles
-5 to 20 °C	240	240	120	1800 (30 months)
0 to 30 °C	240	240	120	1800 (30 months)
10 to 40 °C	240	240	120	1800 (30 months)
20 to 50 °C	240	240	120	1800 (30 months)

Under the Death Valley condition, which can be considered to be an extreme but realistic application condition, both the lead-free board and the tin-lead seemed to survive the given temperature stress condition over a period of 10 years. Figure 4 shows a part of the list of components with their corresponding damage ratio in descending order. Damage ratio indicates the amount of damage accumulated over the entire period of temperature cycling.

It was observed that in Death Valley conditions, the tin-lead board was more susceptible to thermal fatigue than the lead-free board as shown in Figure 3 (snapshot of results as shown in simulation), while in the accelerated condition, the lead-free board was found to be more susceptible than the tin-lead version as shown in Figure 4. This is due to the higher acceleration factor of the lead-free failure model. This is to say, if at a particular accelerated condition the acceleration factor of tin-lead solder is 10, and if the tin-lead interconnect survives x hours in the accelerated conditions, then it is expected to survive 10x hours in the normal usage conditions. The acceleration factors for lead-free solders are generally higher than the tin-lead solders under the same accelerated conditions. Acceleration factor is a function of testing condition and hence changes based on our testing conditions.

Components	Quantity	Failure Model	No. of cycles to failure	Failure Indicator
D10-solder-open	1	1ST_TF_LL_NEW	> Specified (DR:0.72)	View
D41-solder-open	1	1ST_TF_LL_NEW	> Specified (DR:0.72)	View
D18-solder-open	1	1ST_TF_LL_NEW	> Specified (DR:0.72)	View
D12-solder-open	1	1ST_TF_LL_NEW	> Specified (DR:0.71)	View
D20-solder-open	1	1ST_TF_LL_NEW	> Specified (DR:0.71)	View
D4-solder-open	1	1ST_TF_LL_NEW	> Specified (DR:0.70)	View
D36-solder-open	1	1ST_TF_LL_NEW	> Specified (DR:0.70)	View
D3-solder-open	1	1ST_TF_LL_NEW	> Specified (DR:0.69)	View
D22-solder-open	1	Tin-lead	> Specified (DR:0.69)	View
D21-solder-open	1		> Specified (DR:0.68)	View

Components	Quantity	Failure Model	No. of cycles to failure	Failure Indicator
D41-solder-open	1	1ST_TF_LL_NEW	< Specified (DR:1.04)	View
D10-solder-open	1	1ST_TF_LL_NEW	< Specified (DR:1.04)	View
D18-solder-open	1	1ST_TF_LL_NEW	< Specified (DR:1.04)	View
D12-solder-open	1	1ST_TF_LL_NEW	< Specified (DR:1.01)	View
D20-solder-open	1	1ST_TF_LL_NEW	> Specified (DR:0.99)	View
D4-solder-open	1	1ST_TF_LL_NEW	> Specified (DR:0.98)	View
D36-solder-open	1	1ST_TF_LL_NEW	> Specified (DR:0.97)	View
D3-solder-open	1	Lead free	> Specified (DR:0.93)	View
D22-solder-open	1		> Specified (DR:0.92)	View

Figure 3 A Sample of Damage Ratio of Components Under Temperature Cycling

In all the temperature cycling conditions, the parts that were found to be the most susceptible to failure by solder joint cracking in both lead-free and tin-lead boards were ceramic surface mount parts (voltage suppressors) and the ceramic surface mount capacitors.

Components	Quantity	Failure Model	No. of cycles to failure	Failure Indicator
D10-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.54)	View
D41-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.54)	View
D18-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.54)	View
D12-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.53)	View
D20-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.53)	View
D4-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.52)	View
D36-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.52)	View
D3-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.51)	View
D22-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.51)	View
D11-solder-open	4	Tin-lead	> Specified (DR:0.50)	View
D21-solder-open	4		> Specified (DR:0.50)	View

D41-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.21)	View
D10-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.21)	View
D18-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.21)	View
D12-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.20)	View
D20-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.20)	View
D4-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.19)	View
D36-solder-open	4	1ST_TF_LL_NEW	> Specified (DR:0.19)	View
C55-solder-open	4	Lead-free	> Specified (DR:0.18)	View

Figure 4 A Sample of Damage Ratio of Components Under Temperature Cycling

For *vibration analysis*, we adopted truck transportation vibration standard MIL-STD-810, method 514.6-annex C [13]. Figure 5 shows the vibration profile for different direction of random vibration with different values of rms value of g. Vertical direction

profile with an rms value of 1.04g was selected. Table 5 shows the frequency points and corresponding PSD values for the chosen transverse direction.

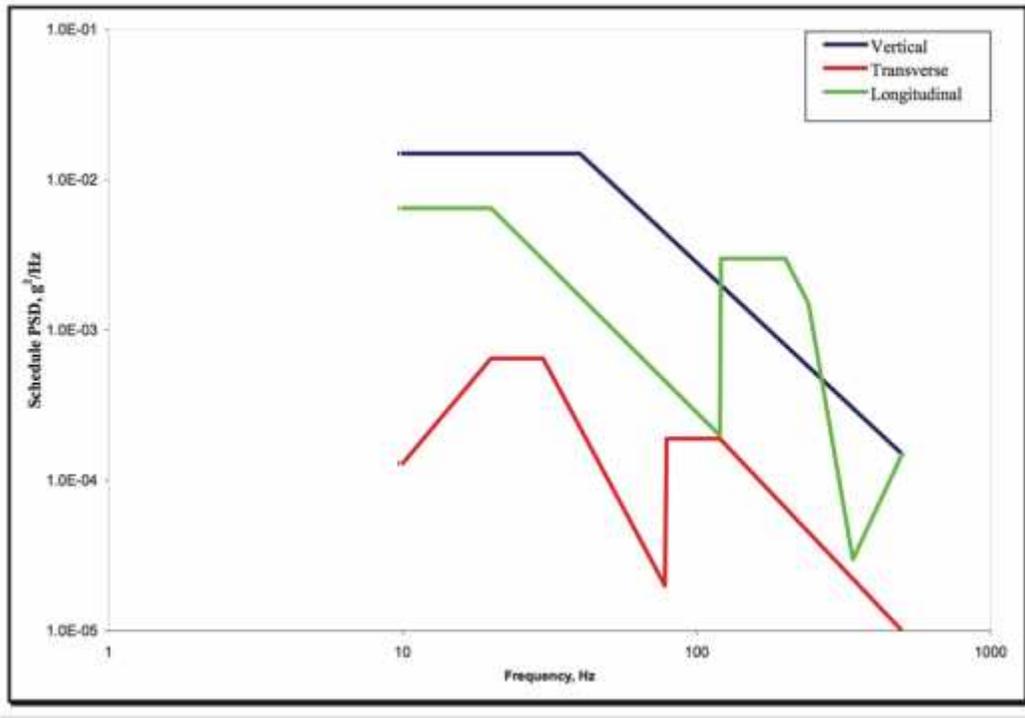


Figure 5 US Highway Truck Vibration Exposure [13]

Table 5 Frequency vs. PSD for Transverse Direction

Frequency (Hz)	PSD (G ² /Hz)
10	0.015
40	0.015
500	0.00015

Figure 6 shows that none of the components experience open failure at interconnects due to the applied vibration. However, it has to be noted that the ceramic components assembled on the board can fail at the component level under vibration even if the interconnects remain intact for high curvature conditions. However, the curvatures estimated for the vibration conditions are not high enough to cause such cracking.

Components	Quantity	Failure Model	Life (DR at 10 years)	Indicator
C42-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
Q1-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
C41-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
Q2-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
Q3-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
C43-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
Q4-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
Q5-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
Q7-interconnect-open	1	Tin-lead	> Specified (DR:0.00)	View
Q8-interconnect-open	1	Tin-lead	> Specified (DR:0.00)	View

Components	Quantity	Failure Model	Life (DR at 10 years)	Indicator
C42-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
Q1-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
C41-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
Q2-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
Q3-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
C43-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
Q4-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
Q5-interconnect-open	1	1ST_VF_RM	> Specified (DR:0.00)	View
Q7-interconnect-open	1	Lead-free	> Specified (DR:0.00)	View
Q8-interconnect-open	1	Lead-free	> Specified (DR:0.00)	View

Figure 6 Results of Vibration Analysis

Tin Whiskers: Tin whiskers are filamentary growths that spontaneously grow from electroplated tin surfaces. Whisker growth starts after an incubation period that varies from seconds to years. Whisker diameters range between 0.006 and 10 μm [14]. Tin whiskers are spontaneous growths from tin and high tin content alloy finishes. Growth can take on a variety of shapes. Whisker lengths can range from a few microns to over 1 mm. Diameters range from less than 1 μm to about 6 μm .

Tin whisker risk must be assessed based on product, application, and tolerance to failure. The risk of tin whisker shorts was estimated using CalceTinWhiskerRisk calculator. Tin whisker risk assessment involves identification of potential whisker failure sites, which are adjacent conductor pairs with at least one surface coated with pure tin or a Pb-free tin finish. The other factors to be considered are the characteristics of whiskers itself - whisker density and whisker length. Any mitigation processes employed such as conformal coating, solder dipping and appropriate part selection should also be considered while assessing these risks.

CalceTinWhisker risk calculator assumes: full surface area of a conductor is susceptible to whisker formation; shortest distance between conductors form the whisker bridging; and whisker growth can be extrapolated from measured data. Failure occurs when $l_w \geq l_s$, where l_w is the length of a whisker and l_s is the spacing between the two adjacent conductors. Because whiskers have been observed to change orientation, the growth angle is no longer considered. Based on the CALCE calculator (after 10,000 iterations), the probability for system failure due to tin whisker short was estimated to be 0.03% (refer to attached

spreadsheet). Components with the highest probability of tin whisker shorting were found to be surface mount leaded ICs and surface mount electrolytic capacitors (with bent lead).

Other Reliability Concerns: Based on the lifecycle conditions that the electronic assembly is subjected to, there can be other potential failure mechanisms that can lead to system failure. Electrochemical migration can be a serious concern due to the mobility of silver ions under humid conditions [15][16]. Stiffness of SAC solders as compared to tin-lead can cause pad cratering under mechanical vibrations. Some gaseous and sultry environments can lead to solder corrosion. However, lead-free solders have been found to be on par or better than tin-lead solders in corrosion resistance [17].

Conclusion: Temperature cycling stress simulation was conducted for three different condition – accelerated condition, approximate application condition, and board rating condition. There were no significant difference between the damage accumulated in the tin-lead interconnects and lead-free interconnects. Accelerated conditions showed lead-free board accumulating marginally more damage than tin-lead due to the higher acceleration factor in the failure model, while the normal usage conditions showed lead-free board to be marginally safer than tin-lead board. Vibration analysis was conducted based on U.S. truck transportation vibration testing standard MIL-STD-810. It was found that lead-free interconnects and tin-lead interconnects showed similar (no damage accumulation) damage accumulation due to the applied vibration condition. It has to be noted, however, that, although the interconnects themselves might not have failed, brittle material components such as ceramic capacitors and diodes might crack under mechanical vibrations.

Tin whisker risk assessment was conducted for the worst-case scenario: Pure tin coating over copper leads, no conformal coating applied. The CALCE tin whisker risk calculator estimated the probability of failure of the system due to tin whisker shorting over a period of 10 years to be 0.3%. Other reliability concerns such as popcorning, ECM, solder corrosion, and pad cratering related to adopting lead-free materials in electronics assembly were briefly discussed.

Apart from these reliability concerns, there has to be continual monitoring on certain features of products such as lead temperature rating, MSL rating, and part temperature rating. All these are critical while selecting the reflow profile and storage conditions. Any deviation between the rated parameters and followed assembly and storage practice can increase the risks of defects and failures of lead-free systems.

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